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(54)Title of the Invention: A Method for Manufacturing A Semiconductor Integrated Circuit Apparatus
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SPECIFICATION

1. Title of the Invention

A Method for Manufacturing A Semiconductor Integrated Circuit Apparatus

2. Claims

1. A method for manufacturing a semiconductor integrated circuit apparatus wherein a semiconductor integrated circuit apparatus is manufactured by forming a monocrystal semiconductor film on an insulation film, and the above method being characterized in comprising a step for forming a slot on a semiconductor substrate, a step for forming an insulation film on at least the surface of the above semiconductor substrate in the above slot so that the above semiconductor substrate should be exposed to one side wall of the above slot, a step for forming a metallic film on the surface of the above semiconductor substrate that is exposed to the side wall of the above slot, a step for forming a semiconductor film on the above insulation film and the above metallic film, and a step for solid phase epitaxial growth of the above monocrystal semiconductor film including a metallic atom to configure the above metallic film on the above insulation film by

heating at a specified temperature cycle.

2. A method for manufacturing a semiconductor integrated circuit apparatus of claim 1, wherein the conductive type of the above semiconductor substrate is different from that of the above monocrystal semiconductor film.

3. A method for manufacturing a semiconductor integrated circuit apparatus of claim 2, wherein the conductive type of the above semiconductor substrate is n-type, while that of the above monocrystal semiconductor film is p-type.

4. A method for manufacturing a semiconductor integrated circuit apparatus of one of claims 1 to 3, wherein the above semiconductor substrate is an Si substrate, while the above semiconductor film is a polycrystal Si film.

5. A method for manufacturing a semiconductor integrated circuit apparatus of one of claims 1 to 4, wherein the above metallic film is an Al substrate.

6. A method for manufacturing a semiconductor integrated circuit apparatus of one of claims 1 to 5, wherein the above monocrystal semiconductor film is a p-type monocrystal Si film including Al up to solid solution limit.

7. A method for manufacturing a semiconductor integrated circuit apparatus of one of claims 1 to 6, wherein the above semiconductor integrated circuit apparatus is a CMOSLSI.

3. Detailed Description of the Invention

[Field of the Invention]

The present invention relates to a method for manufacturing a semiconductor integrated circuit apparatus, more specifically, relates to a technology useful for application for forming a monocrystal semiconductor film on an insulation film.

[Prior Art]

In the conventional CMOS technology, an n well is formed in a p-type semiconductor substrate or a p well is formed in an n-type semiconductor substrate (for example, Tokuyama and Hashimoto, "MOSLSI Manufacturing Technology" (Nikkei Macglowhill, June 20, 1985) p.40).

[Problems to be Solved by the Invention]

However, in this case, a semiconductor substrate and an n well or a

p well are not separated with an insulation film, as a result, there has been a problem that it is difficult to prevent the occurrence of what is called latch-up.

It is an object of the present invention to provide a technology that enables to form easily a desired conductive type monocrystal semiconductor film in a status separate from a semiconductor substrate with an insulation film.

The above and other objects and innovative characteristics of the present invention will be made clear in the descriptions herein and the attached drawings.

[Means to Solve the Problems]

As an electrode wiring raw material in a semiconductor integrated circuit apparatus, an Al film with addition of Si (silicon) by for example 1 to 3 weight % is employed in general. The present inventor has found that when an Al film with addition of Si is formed on a Si substrate, Si in the above Al film goes through solid solution epitaxial growth on the above Si substrate by heating process in a manufacture of a semiconductor integrated circuit apparatus, and as a result, a p-type monocrystal Si film that includes Al up to solid solution limit is obtained, and led to the present invention.

The outline of the representative one of the inventions disclosed in the present application is described hereinafter.

Namely, the present invention embodies the steps for forming a slot on a semiconductor substrate, for forming an insulation film on at least the surface of the above semiconductor substrate in the above slot so that the above semiconductor substrate should be exposed to one side wall of the above slot, for forming a metallic film on the surface of the above semiconductor substrate that is exposed to the side wall of the above slot, for forming a semiconductor film on the above insulation film and the above metallic film, and for solid phase epitaxial growth of the above monocrystal semiconductor film including a metallic atom to configure the above metallic film on the above insulation film by heating at a specified temperature cycle.

[Action]

According to the means mentioned above, metallic atoms to configure a metallic film are taken in a semiconductor film at epitaxial growth, so a kind of metals is selected appropriately, thereby it is possible to easily form a desired conductive type monocrystal

semiconductor film in a status separated from a semiconductor substrate with an insulation film.

[Embodiment]

In reference to drawings, structures according to the present invention are described below in details on the basis of an embodiment.

By the way, in all the drawings, identical codes are allotted to components having identical function, and their repeated explanations are omitted hereinafter.

As shown in FIG. 1, first for example, a slot 2 with a rectangular cross section is formed on the surface of a semiconductor substrate 1 such as for example an n-type Si substrate, thereafter, an insulation film 3 such as for example an SiO_2 film is formed on the surface of this semiconductor substrate 1 by for example thermal oxidation method, then a portion positioned at one side wall 2a of the slot 2 in this insulation film 3 is selectively etched and removed, and the above semiconductor substrate 1 is exposed to this portion. Thereafter, an Al film 4 is formed on the whole surface, and other portions than the portion positioned at the side wall 2a of the above slot 2 among this Al film 4 are etched and removed. Thereafter, for example by CVD method, for example a polycrystal Si film 5 is formed all over the surface.

Then, in this status, heating is carried out at a temperature cycle in a specified temperature range, for example, as shown in FIG.6, at a temperature cycle A between 100°C and 50°C. As for the temperature cycle A, increasing temperature is carried out relatively fast, while decreasing temperature is carried out gradually, and for example, the time intervals of t1, t2, and t3 in FIG.6 are set 5 to 10 minutes, 10 minutes, and 30 to 40 minutes, respectively. By the way, this temperature cycle may be for example a sine wave temperature cycle.

And when heating is carried out at this temperature cycle A, as is seen from the Al-Si system condition drawing shown in FIG.6, the solid solution degree of Si in the above Al film 4 fluctuates with time t as shown in the curved line B. Namely, at increasing temperature, the solid solution degree of Si in the Al film 4 increases, while at decreasing temperature, it decreases. In this case, since the stability of the above polycrystal Si film 5 is lower (whose free energy is greater) and more active than the above semiconductor substrate 1, at increasing temperature, the Al film 4 absorbs Si from the polycrystal Si film 5 adjacent thereto, and at decreasing temperature, Si in this Al film 4 goes

through solid solution epitaxial growth on the surface of the semiconductor 1 at the side wall 2a of the slot 2. This epitaxial growth proceeds in the direction parallel with the surface of the semiconductor substrate 1, as the Al film 4 goes to the opposite side to the side wall 2a as the above temperature cycle A. As a consequence, through a process as shown in FIG. 2, and as shown in FIG. 3, on the insulation film 3 in the slot 2, a p-type monocrystal Si film 6 that includes Al atoms up to solid solution limit is formed. Thereby, it is possible to easily form a p-type monocrystal Si film 6 on the insulation film 3 in a status separated from the semiconductor substrate 1, without impurity doping by ion implementation or so. And further, it is possible to make the surface of this p-type monocrystal Si film 6 at almost the same level as the surface of the semiconductor substrate 1, thus there is no step, so that it is very advantageous for later processes.

In the next place, both the ends of the polycrystal Si film 5 and the p-type monocrystal Si film and the Al film 4 are etched and removed, and a status shown in FIG. 4 appears.

Thereafter, as shown in FIG. 5, an insulation film 7 such as for example an SiO_2 film is formed all over the surface by for example CVD method, thereafter etching is carried out all over the surface, thereby the above insulation film 7 is filled in between the p-type monocrystal Si film 6 and the side wall of the slot 2. Then, a gate insulation film 8 such as for example an SiO_2 film is formed on the surface of the above p-type monocrystal Si film 6 by for example thermal oxidation method, and further, a gate electrode 9 such as for example a polycrystal Si film, for example an n^+ type source area 10 and a drain area 11 are formed, and an n channel MOSFET 12 is formed. Thereafter, a gate electrode 9 such as for example a polycrystal Si film is formed on the insulation film 3, and further, a p^+ type source area 13 and a drain area 14 are formed in the semiconductor substrate 1, and a p channel MOSFET 15 with the insulation film 3 as a gate insulation film is formed, thereby the objective CMOSLSI is completed.

In a CMOSLSI according to the present preferred embodiment having above mentioned structure, as mentioned previously, the semiconductor substrate 1 and the p-type monocrystal Si film 6 are separated from each other with an insulation film 3, it is possible to effectively prevent the occurrence of latch-up, and also it is possible to reduce parasitic capacity.

Heretofore explained in concrete is the present invention by the inventor in reference to the above preferred embodiment. and it is taken for granted that the present invention is not limited solely to the above preferred embodiment. and the present embodiment is therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

For example, the present invention may be applied to the manufacture of other various semiconductor integrated circuit apparatus than CMOSLSI.

[Effect of the Invention]

The effect obtained by the representative one of the inventions disclosed in the present application may be briefly explained as below.

Namely, it is possible to easily form a desired conductive type monocrystal semiconductor film in a status separated from a semiconductor substrate by an insulation film.

4. Brief Description of the Drawings

Figs. 1 to 5 are cross sections showing processes of the method for manufacturing a CMOSLSI according to one preferred embodiment under the present invention.

Fig. 6 is a schematic diagram showing an Al-Si system condition drawing and a diagram showing fluctuations of the solid solution degree of Si by temperature cycle.

In the figures. the codes represent the followings:

1	Semiconductor substrate
2	Slot
3, 7	Insulation film
4	Metallic film
5	Polycrystal Si film (semiconductor film)
6	P-type monocrystal Si film (monocrystal semiconductor film)
8	Gate insulation film
9	Gate electrode
10, 13	Source area
11,14	Drain area
12	n channel MOSFET
15	p channel MOSFET

Agent Patent Lawyer Michio Ogawa

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WPI Acc No: 1988-039523/198806
Mfg. single crystal semiconductor film on insulating film - by leading metal atoms to semiconductor film during simple epitaxial growth process
NoAbstract Dwg 1-4/6
Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
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㊹発明の名称　半導体集積回路装置の製造方法

㉑特　願　昭61－140060

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明細書

1．発明の名称

半導体集積回路装置の製造方法

2．特許請求の範囲

1．絶縁膜上に単結晶半導体膜を形成することにより半導体集積回路装置を製造するようにした半導体集積回路装置の製造方法であって、半導体基板に溝を形成する工程と、前記溝の一方の側壁に前記半導体基板が露出するように少なくとも前記溝内の前記半導体基板の表面に絶縁膜を形成する工程と、前記溝の側壁に露出している前記半導体基板の表面に金属膜を形成する工程と、前記絶縁膜及び前記金属膜の上に半導体膜を形成する工程と、所定の温度サイクルによる加熱を行うことにより、前記絶縁膜上に前記金属膜を構成する金属原子を含む前記単結晶半導体膜を固相エピタキシャル成長させる工程とをそれぞれ具備することを特徴とする半導体集積回路装置の製造方法。

2．前記半導体基板の導電型と前記単結晶半導体膜の導電型とが互いに異なることを特徴とする特許請求の範囲第1項記載の半導体集積回路装置の製造方法。

3．前記半導体基板の導電型がn型であり、前記単結晶半導体膜の導電型がp型であることを特徴とする特許請求の範囲第2項記載の半導体集積回路装置の製造方法。

4．前記半導体基板がSi基板であり、前記半導体膜が多結晶Si膜であることを特徴とする特許請求の範囲第1項－第3項のいずれか一項記載の半導体集積回路装置の製造方法。

5．前記金属膜がAl膜であることを特徴とする特許請求の範囲第1項～第4項のいずれか一項記載の半導体集積回路装置の製造方法。

6．前記単結晶半導体膜がAlを固溶限度まで含んでいるp型単結晶Si膜であることを特徴とする特許請求の範囲第1項～第5項のいずれか一項記載の半導体集積回路装置の製造方法。

7．前記半導体集積回路装置がCMOSLSIであることを特徴とする特許請求の範囲第1項－

第６項のいずれか一項記載の半導体集積回路装置の製造方法．

３．発明の詳細な説明

〔産業上の利用分野〕

本発明は，半導体集積回路装置の製造方法に関し，特に，絶縁膜上に単結晶半導体膜を形成するのに適用して有効な技術に関するものである．

〔従来の技術〕

従来のＣＭＯＳ技術では，ｐ型半導体基板中にｎウエルを形成するか又はｎ型半導体基板中にｐウエルを形成している（例えば，菅山，樋本編著「ＭＯＳＬＳＩ製造技術」（日経マグロウヒル社，1985年6月20日発行）p.40）．

〔発明が解決しようとする問題点〕

しかしながら，この場合には，半導体基板とｎウエル又はｐウエルとが絶縁膜で分離されておらず，このためいわゆるラッチアップの発生を防止するのが難しいという問題があった．

本発明の目的は，絶縁膜により半導体基板と分離された状態で所望の導電型の単結晶半導体膜を容易に形成することが可能な技術を提供することにある．

本発明の前記ならびにその他の目的と新規な特徴は，本明細書の記述及び添付図面によって明らかになるであろう．

〔問題点を解決するための手段〕

半導体集積回路装置における電極配線材料としては，通常，Si(シリコン)が例えば１～３重量％添加されたAl膜が用いられている．本発明者は，このようなSiが添加されたAl膜をSi基板上に形成した場合，半導体集積回路装置の製造工程における熱処理によって前記Al膜中のSiが前記Si基板上に固相エピタキシャル成長して，Alを固溶限度まで含んでいるｐ型単結晶Si膜が得られることを見い出し，本発明を案出するに到った．

本願において開示される発明のうち，代表的なものの概要を説明すれば，下記のとおりである．

すなわち，半導体基板に溝を形成する工程と，前記溝の一方の側壁に前記半導体基板が露出するように少なくとも前記溝内の前記半導体基板の表面に絶縁膜を形成する工程と，前記溝の側壁に露出している前記半導体基板の表面に金属膜を形成する工程と，前記絶縁膜及び前記金属膜の上に半導体膜を形成する工程と，所定の温度サイクルによる加熱を行うことにより，前記絶縁膜上に前記金属膜を構成する金属原子を含む単結晶半導体膜を固相エピタキシャル成長させる工程とをそれぞれ具備している．

〔作　用〕

上記した手段によれば，金属膜を構成する金属原子がエピタキシャル成長時に半導体膜中に取り込まれるので，金属の種類を適当に選択することにより，絶縁膜により半導体基板と分離された状態で所望の導電型の単結晶半導体膜を容易に形成することができる．

〔実施例〕

以下，本発明の構成について，一実施例に基づき図面を参照しながら説明する．

なお，全図において，同一の機能を有するものには同一の符号を付け，その繰り返しの説明は省略する．

第１図に示すように，まず例えばｎ型Si基板のような半導体基板１の表面に例えば矩形断面の溝２を形成し，次いでこの半導体基板１の表面に例えば熱酸化法により例えばSiO_2膜のような絶縁膜３を形成した後，この絶縁膜３のうちの溝２の一方の側壁２ａに位置する部分を選択的にエッチング除去してこの部分に前記半導体基板１を露出させる．次に全面にAl膜４を形成した後，このAl膜４のうちの前記溝２の側壁２ａに位置する部分のみを残してその他の部分をエッチング除去する．この後，全面に例えばＣＶＤ法により例えば多結晶Si膜５を形成する．

次にこの状態で，所定の温度範囲での温度サイクル，例えば第６図に示すように１００℃と５００℃との間の温度サイクルＡによる加熱を行う．この温度サイクルＡは，例えば昇温は比較的速く行い，降温は徐々に行うように選び，例えば第６図の各時間間隔t_1，t_2，t_3をそれぞれ例えば５～１０分，１０分，３０～４０分に選択する．

なおこの温度サイクルは、例えば正弦波的な温度サイクルとすることも可能である。

この温度サイクルAによる加熱を行うと、第6図に示すAl-Si系状態図からわかるように、前記Al膜4中のSiの固溶度も時間tと共に曲線Bで示すように変動する。すなわち、昇温時にはAl膜4中のSiの固溶度は増加し、降温時には減少する。この場合、前記半導体基板1よりも前記多結晶Si膜5の方が安定度が低く（自由エネルギーが大きい）て活性であるため、昇温時にAl膜4はこれに接している多結晶Si膜5からSiを吸収し、降温時にはこのAl膜4中のSiが溝2の側壁2aにおける半導体基板1の表面に固相エピタキシャル成長する。このようなエピタキシャル成長が、前記温度サイクルAと共にAl膜4が側壁2aと反対側に移動しつつ、半導体基板1の表面に平行な方向に順次進行する。この結果、第2図に示すような過程を経て、第3図に示すように、溝2内の絶縁膜3上に、Al原子を固溶限度まで含んだp型単結晶Si膜6が形成される。これによって、イオン打ち込み等による不純物ドーピングを行うことなく、半導体基板1と分離された状態で絶縁膜3上にp型単結晶Si膜6を容易に形成することができる。しかも、このp型単結晶Si膜6の表面を半導体基板1の表面とほぼ同一の高さにすることができるので、段差がなく、後の工程を進める上で有利である。

次に多結晶Si膜5、p型単結晶Si膜6の両端部及びAl膜4をエッチング除去して、第4図に示す状態とする。

次に第5図に示すように、例えばCVD法により全面に例えばSiO_2膜のような絶縁膜7を形成した後、全面エッチングを行うことにより、p型単結晶Si膜6と溝2の側壁との間を前記絶縁膜7で埋めた構造とする。次に、前記p型単結晶Si膜6の表面に例えば熱酸化法により例えばSiO_2膜のようなゲート絶縁膜8を形成し、さらに例えば多結晶Si膜のようなゲート電極9、例えばn^+型のソース領域10及びドレイン領域11を形成して、nチャネルMOSFET12を形成する。この後絶縁膜3上に例えば多結晶Si膜のようなゲート電極9を形成し、さらに半導体基板1中に例えばp^+型のソース領域13及びドレイン領域14を形成して、絶縁膜3をゲート絶縁膜とするpチャネルMOSFET15を形成し、これによって目的とするCMOSLSIを完成させる。

上述のように構成された本実施例によるCMOSLSIにおいては、既述のように半導体基板1とp型単結晶Si膜6とが絶縁膜3により互いに分離されているので、ラッチアップの発生を効果的に防止することができると共に、寄生容量の低減を図ることができる。

以上、本発明者によってなされた発明を前記実施例に基づき具体的に説明したが、本発明は前記実施例に限定されるものではなく、その要旨を逸脱しない範囲において種々変形し得ることは勿論である。

例えば、本発明は、CMOSLSI以外の各種半導体集積回路装置の製造に適用することが可能である。

〔発明の効果〕

本願において開示される発明のうち、代表的なものによって得られる効果を簡単に説明すれば、下記のとおりである。

すなわち、絶縁膜により半導体基板と分離された状態で所望の導電型の単結晶半導体膜を容易に形成することができる。

4．図面の簡単な説明

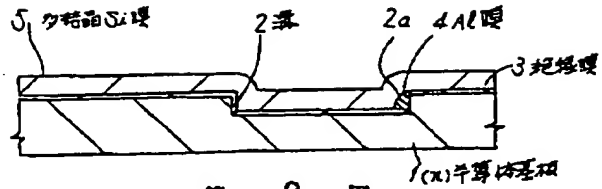
第1図～第5図は、本発明の一実施例によるCMOSLSIの製造方法を工程順に示す断面図、

第6図は、Al-Si系状態図及び温度サイクルによるSiの固溶度の変動を示す図である。

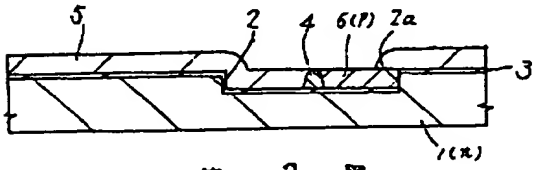
図中、1…半導体基板、2…溝、3、7…絶縁膜、4…金属膜、5…多結晶Si膜（半導体膜）、6…p型単結晶Si膜（単結晶半導体膜）、8…ゲート絶縁膜、9…ゲート電極、10、13…ソース領域、11、14…ドレイン領域、12…nチャネルMOSFET、15…pチャネルMOSFETである。

代理人　弁理士　小川勝男

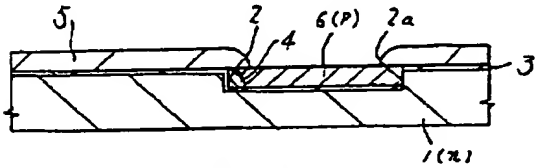
第 1 図



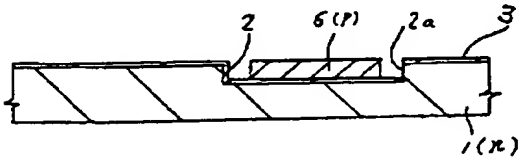
第 2 図



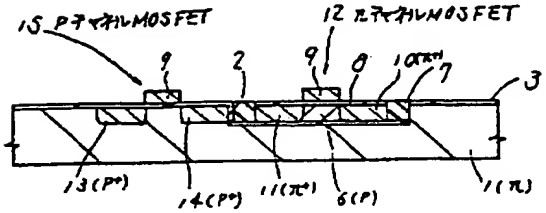
第 3 図



第 4 図



第 5 図



第 6 図